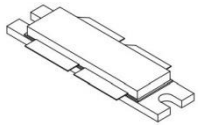
MQ1380VP LDMOS TRANSISTOR

Document Number: MQ1380VP
Preliminary Datasheet V2.0

1000W, 50V High Power RF LDMOS FETs

MQ1380VP



Description

The MQ1380VP is a 1000-watt, high performance, internally matched LDMOS FET, designed for multiple applications with frequencies 0.7 to 1.1GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as Avionics applications.

It is recommended to use this device under pulse condition. Please ensure adequate cooling if running at CW

- Typical **short pulse** Performance (on innogration 915MHz narrow band test fixture with device soldered): Pulse width:100uS, duty cycle: 10%, Vds = 50 V, Idq = 100 mA, TA = 25 C

Freq (MHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Ids (A)	Eff (%)
915	40.3	59.23	838	18.9	2.977	58.02
915	41.3	59.68	929	18.4	3.228	59.21
915	42.3	60.04	1009	17.7	3.445	60.16
915	43.3	60.32	1076	17.0	3.638	60.68
915	44.3	60.54	1132	16.2	3.806	60.95
915	45.3	60.72	1180	15.4	3.953	61.11
915	46.3	60.86	1219	14.6	4.078	61.13

- Typical **long pulse** Performance (on innogration 915MHz narrow band test fixture with device soldered): Vds = 50 V, Idq = 100 mA, TA = 25 C

Freq (MHz)	Pin (dBm)	pulse width (ms)	pulse period（ms)	duty cycel (%)	Pout (dBm)	Pout (W)	Gain (dB)	Ids (A)	Eff (%)
915	46.3	1.0	10.0000	10.0	60.49	1119	14.2	3.9	58.76
915	46.3	1.0	5.0000	20.0	60.33	1079	14.0	7.6	57.39
915	46.3	1.0	3.3333	30.0	60.32	1076	14.0	11.3	57.50
915	46.3	1.0	2.5000	40.0	60.34	1081	14.0	15.2	57.14
915	46.3	1.0	2.0000	50.0	60.32	1077	14.0	18.9	57.11
915	46.3	1.0	1.6667	60.0	60.28	1066	14.0	22.5	56.97
915	46.3	1.0	1.4286	70.0	60.20	1047	13.9	25.8	56.87
915	46.3	1.0	1.2500	80.0	60.11	1025	13.8	29.2	56.23

- Typical **Avionics** Performance (on innogration narrow band test fixture with device soldered):

Frequency:1030MHz,: Vds = 50 Volts, Idq = 100 mA, TA = 25 C

Pulse condition	Gp (dB)	P_{OUT}(W)	η_D@P_{OUT} (%)
pulse width 100us duty cycle 10%	14.5	1100	56
pulse width 50us duty cycle 1%	14	1200	56.5

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Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C, 1000W Pout, Pulse width: 100us, duty cycle: 10%, Vds=50 V, IDQ = 100 mA , Frequency at 915MHz	RθJC	0.02	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	115	——	——	V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$	——	1.6	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.0		V

Functional Tests (In Innogration test fixture, 50 ohm system) : V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f = 915 MHz, Pulse CW Signal Measurements.

(Pulse Width=100 μs, Duty cycle=10%)

Power Gain	Gp	———	17.7	———	dB
Output Power	P_{out}		1000	———	W
Drain Efficiency@P1dB	η_D	———	60	———	%
Input Return Loss	IRL	———	-7	———	dB

Figure1 915MHz Pulsed CW gain and efficiency as a Function of Output Power

Pulse width 100us and duty cycle 10%

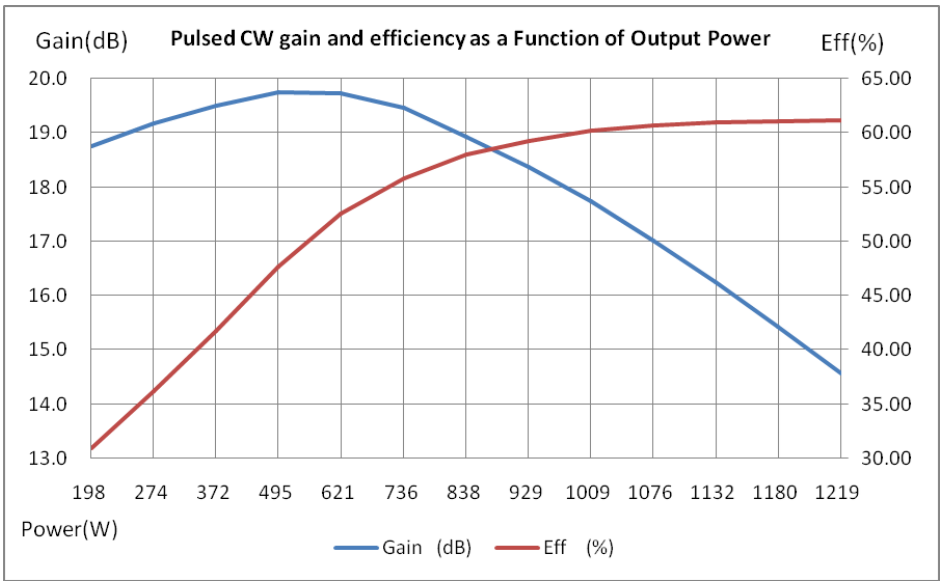


Figure 2: 915MHz output power and efficiency as a Function of duty cycle

Pulse width=1ms Pin=46.3dBm

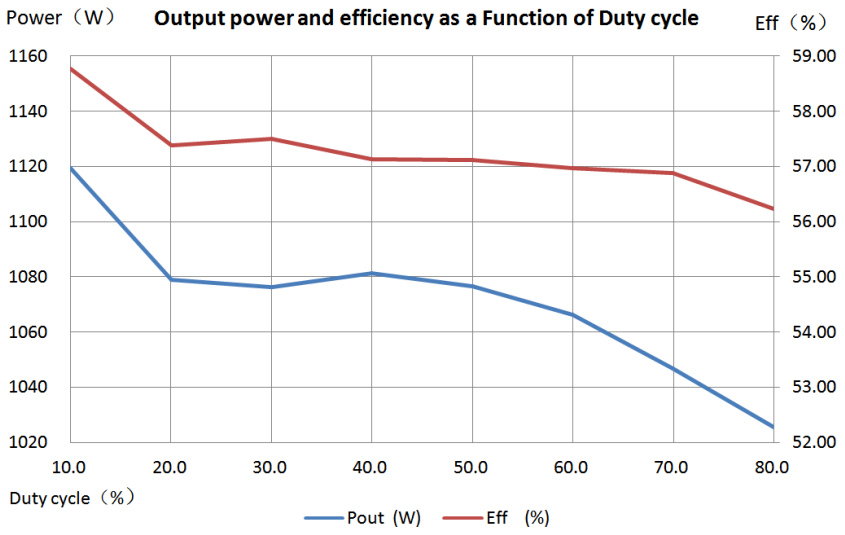


Figure 3: 1030MHz Pulsed CW gain and efficiency as a Function of Output Power

Pulse width 100us and duty cycle 10%

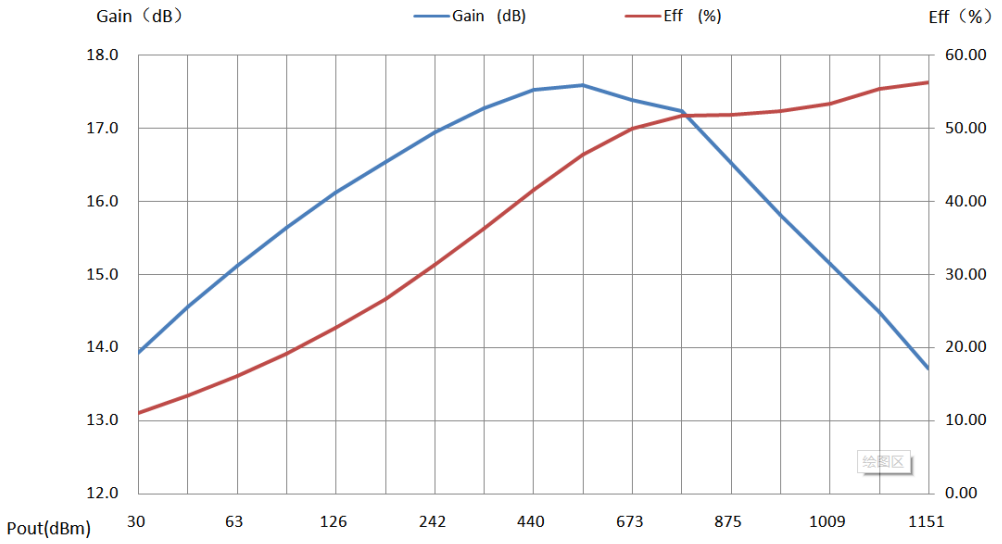
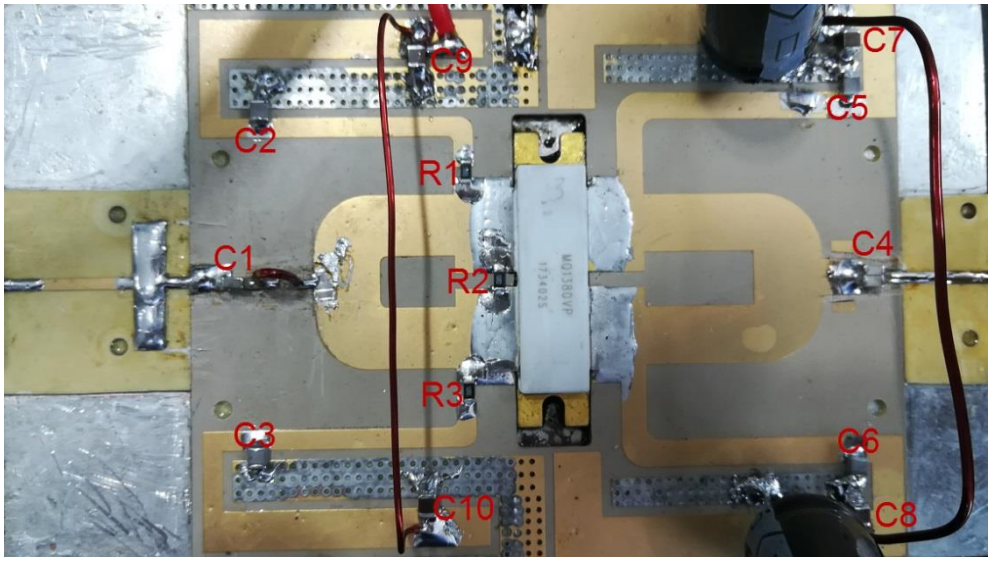
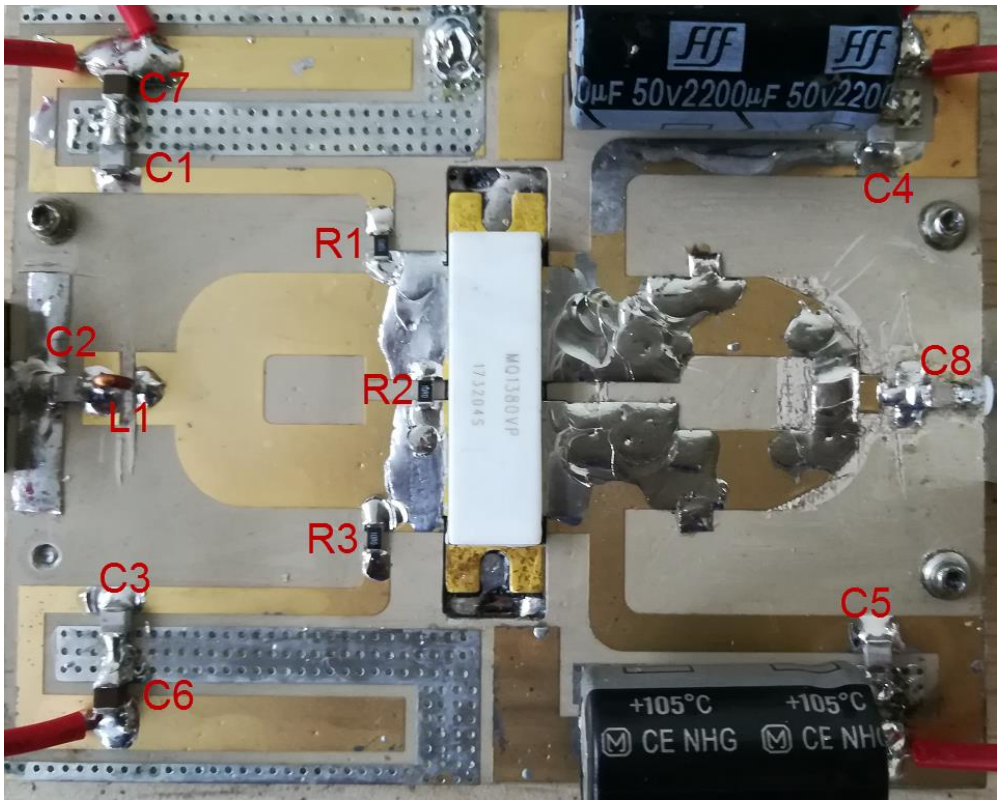


Figure 4: Test fixture photo(915MHz)



BOM of 915MHz fixture (PCB 25mil TC600 from Arlon)		
C1,C2,C3,C5,C6	100PF	ATC800B
C4	27PF x2	ATC800B
c7,C8,C9,C10	10UF	
R1,R2,R3	10Ω	

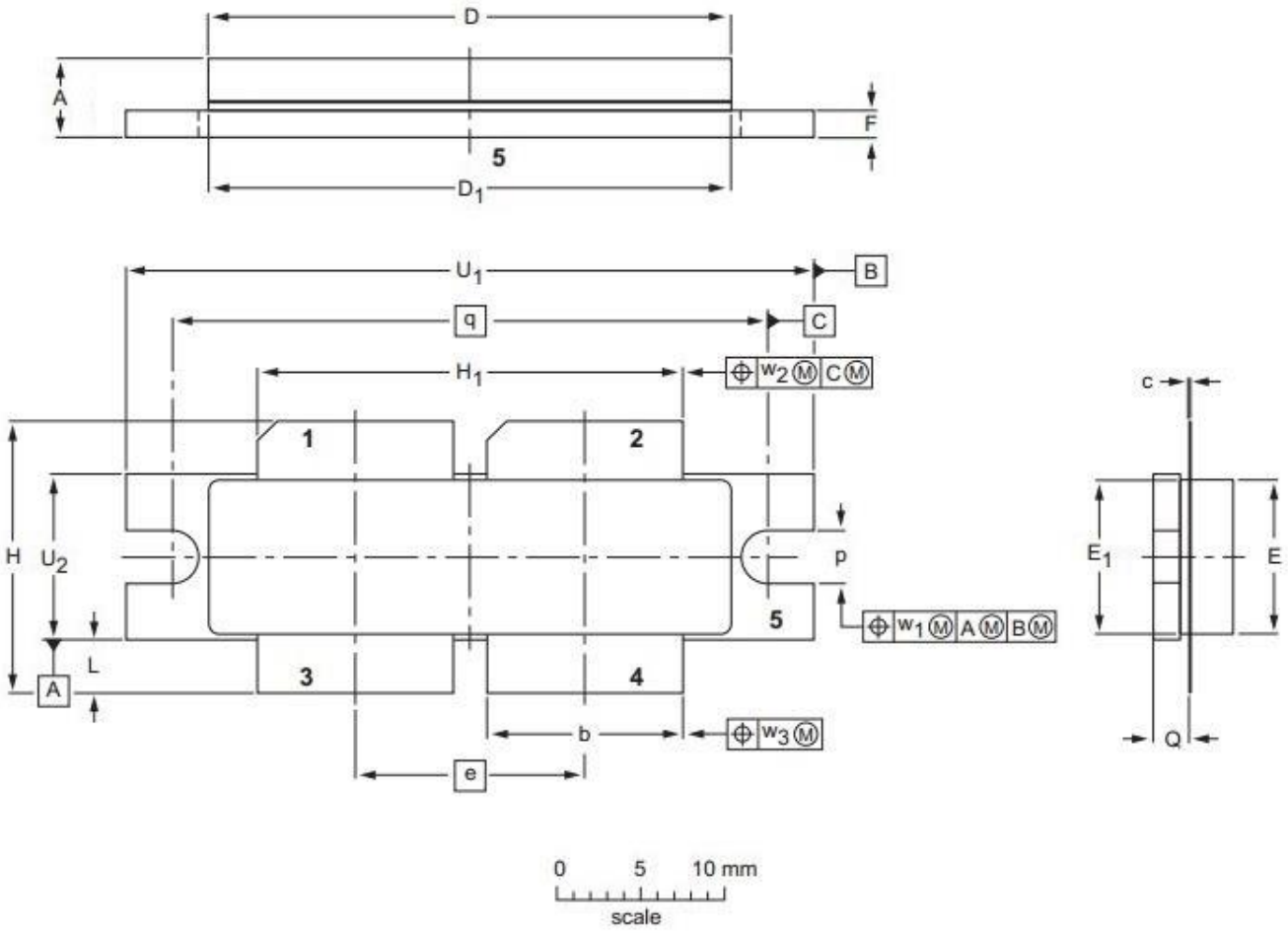
Figure 5: Test fixture photo(1030MHz)



BOM of 1030MHz fixture (PCB 25mil TC600 from Arlon)		
C1,C2,C3,C4,C5,C8	56PF	ATC800B
C6,C7	10UF	
R1,R2,R3	10Ω	
L1	1turns	Diameter=3mm

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2017/09/11	Rev 1.0	Preliminary Datasheet Creation
2017/09/26	Rev 2.0	Modification on the upper frequency band to 1.1GHz

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